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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,279	07/07/2003	Serge F. Fruhauf	02-S-104 (850063.599)	7433

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EXAMINER	
LEE, DIANE I	

ART UNIT	PAPER NUMBER
2876	

DATE MAILED: 03/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/614,279	FRUHAUF, SERGE F.	
	Examiner	Art Unit	
	D. I. Lee	2876	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,9, 12-14, 17-18, 20, 23-24, 27* is/are rejected.

7)☒ Claim(s) *5-8,10,11,15,16,19,21,22,25 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/7/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-27 are presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4, 9, 12-14, 17-18, 20, 23-24 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Feuser et al. [US 6,801,956 B2-referred as Feuser] in view of Poisner et al. [US 6,269,443 B1-referred as Poisner].

Re claim 1: Feuser discloses a smart card apparatus (see Figs. 1 and 2 for example), comprising:

a processor (i.e., CPU, see col. 1, line 60);

a status register (i.e., status register in Fig. 2) coupled to the processor to store status information indicative of a status associated with the processor (see col. 3, lines 1-9 and 44-47); and

control logic (i.e., internal reset circuit in Fig. 2), wherein the control logic can initiate a reset signal (see col. 2, lines 25-31).

Feuser does not expressly teach the control logic is coupled to the processor and to the status register to check the status information stored therein to determine the status of the processor, and wherein if the control logic determines that the status information indicates a non-responsive state associated with the processor, the control logic can initiate the reset signal to the processor to remove the processor from the non-responsive state.

Poisner disclose an apparatus for automatically selecting CPU clock frequency multiplier (See the abstract), wherein a system logic device comprising a control logic (i.e., processor failure detection unit 284 in Fig. 2) is coupled to a processor (i.e., coupled to processor 210 via system bus 225 in Fig. 2) and to a status register (i.e., clock frequency multiplier indicator circuit 285 and non-volatile memory device 270 in Fig. 2) to check a status information stored therein to determine a status of the processor (see col. 3, lines 6-9 and 17-19; in fact, the processor failure detection unit checks to see the processor status if it performs a first instruction fetch from the non-volatile memory device inherently implies a control logic coupled to a processor and to a status register to check a status information stored therein to determine a status of the processor), and wherein if the control logic determines that the status information indicates a non-responsive state associated with the processor (i.e., processor failure is detected; see col. 4, lines 45-47), the control logic (i.e., the processor failure detection unit) can initiate the reset signal (i.e., reset 201 in Fig. 2) to the processor to remove the processor from the non-responsive state (i.e., resetting the processor with making a determination of whether the processor is behaving properly, see col. 3, lines 61-64).

Therefore, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to have included the system logic device, as disclosed by Poisner, in the control logic (i.e., internal reset circuit), as disclosed by Feuser, for the advantage of providing the smart card (i.e., device) for selecting a clock frequency multiplier without the need of human intervention (see col. 2, lines 60-64 of Poisner).

Re claim 2: Feuser teaches the non-responsive state comprises a mute mode (i.e., processor failed status, which means no operation may be performed, see col. 4, lines 50-52).

Re claim 3: Feuser teaches the processor (i.e., CPU, see col. 1, line 60), status register (i.e., status register in Fig. 2), and control logic (i.e., internal reset circuit in Fig. 2) comprise part of a universal serial bus (USB)-compliant smart card (see col. 1, lines 50-56).

Re claim 4: Poisner teaches reset logic (i.e., reset circuitry 281 in Fig. 2) coupled between the control logic (i.e., processor failure detection unit 284 in Fig. 2) and the processor (i.e., processor 210 in Fig. 2) to provide the reset signal (i.e., reset 201 in Fig. 2) to the processor (see col. 3, lines 13-16).

Re claim 9: Feuser discloses a smart card system (see Figs. 1 and 2), comprising: a means for storing processor status information (i.e., status register in Fig. 2, see col. 3, lines 1-9 and 44-47).

Feuser does not expressly teach a means for checking the stored processor status information to determine if a processor has entered a non-responsive mode; and a means for automatically resetting the processor from the non-responsive mode, if the stored processor status information indicates that the processor has entered the non-responsive mode.

Poisner discloses an apparatus for automatically selecting CPU clock frequency multiplier (See Abstract), wherein a system logic device comprising a means for checking the stored processor status information (i.e., processor failure detection unit 284 in Fig. 2) to determine if a processor (i.e., processor 210 in Fig. 2) has entered a non-responsive mode (i.e., if a processor failure is detected, see col. 4, lines 45-47); and a means for automatically resetting the processor (i.e., reset circuit 281 in Fig. 2) from the non-responsive mode (i.e., resetting the processor with making a determination of whether the processor is behaving properly, see col. 3, lines 61-64), if the stored processor status information indicates that the processor has entered the non-responsive mode (i.e., if a processor failure is detected, see col. 4, lines 45-47).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included the system logic device, as disclosed by Poisner, in the smart card system, as disclosed by Feuser, for the advantage of providing the smart card system (i.e., device) for selecting a clock frequency multiplier without the need of human intervention (see col. 2, lines 60-64 of Poisner).

Re claim 12: Feuser teaches a means for resetting the processor based on supplied power (i.e., power-on reset, see col. 2, lines 6-8); and a means for resetting the processor based on a request (i.e., USB reset, see col. 2, lines 42-50).

Re claim 13: Feuser discloses a method usable for smart card system (see Figs. 1 and 2), comprising: storing status information associated with a state of a processor (i.e., status register in Fig. 2, see col. 3, lines 1-9 and 44-47).

Feuser does not expressly teach checking the stored status information to determine if the status information indicates that the processor has entered a non-responsive state; and if the status information indicates that the processor has entered the non-responsive state, automatically resetting the processor to remove it from the non-responsive state.

Poisner discloses a method for automatically selecting CPU clock frequency multiplier (see Abstract), wherein checking a stored status information to determine if the status information indicates that a processor (i.e., processor 210 in Fig. 2) has entered a non-responsive state (i.e., if a processor failure is detected, see col. 4, lines 45-47); and if the status information indicates that the processor has entered the non-responsive state (i.e., if a processor failure is detected, see col. 4, lines 45-47), automatically resetting the processor to remove it from the non-responsive state (i.e., resetting the processor with making a determination of whether the processor is behaving properly, see col. 3, lines 61-64).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied the method, as disclosed by Poisner, to the method usable for smart card, as disclosed by Feuser, for the advantage of providing the smart card (i.e., device) for selecting a clock frequency multiplier without the need of human intervention (see col. 2, lines 60-64 of Poisner).

Re claim 14: Feuser teaches the non-responsive state comprises a mute mode (i.e., the processor failed status is when it is determined that no operation may be performed, thus the process has entered the non-responsive state, see col. 4, lines 50-52).

Re claim 17: Feuser teaches resetting the processor in response to a first signal associated with power supplied to the processor (i.e., power-on reset, see col. 2, lines 6-8); and resetting the processor in response to a specific request received from a host device to reset the processor (i.e., USB reset, see col. 2, lines 42-50).

Re claim 18: Feuser discloses an article of manufacture (i.e., smart card system; see Figs. 1 and 2), comprising: a machine-readable medium having instructions stored thereon (i.e., RAM and ROM memory, see col. 1, lines 60-61) to: store status information associated with a state of a processor (i.e., status register in Fig. 2, see col. 3, lines 1-9 and 44-47).

Feuser does not expressly teach check the stored status information to determine if the status information indicates that the processor has entered a non-responsive state; and automatically reset the processor to remove it from the non-responsive state, if the status information indicates that the processor has entered the non-responsive state.

Poisner discloses a method for automatically selecting CPU clock frequency multiplier (see the abstract), wherein check a stored status information to determine if the status information indicates that a processor (i.e., processor 210 in Fig. 2) has entered a non-responsive state (i.e., if a processor failure is detected, see col. 4, lines 45-47); and automatically reset the processor to remove it from the non-responsive state (i.e., resetting the processor with making a determination of whether the processor is behaving properly, see col. 3, lines 61-64), if the status information indicates that the processor has entered the non-responsive state (i.e., if a processor failure is detected, see col. 4, lines 45-47).

Therefore, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to have implemented the method, as disclosed by Poisner, in the article of

manufacture, as disclosed by Feuser, for the advantage of providing the article (i.e., device) for selecting a clock frequency multiplier without the need of human intervention (see col. 2, lines 60-64 of Poisner).

Re claim 20: Feuser teaches reset the processor in response to a first signal associated with power supplied to the processor (i.e., power-on reset, see col. 2, lines 6-8); and reset the processor in response to a specific request received from a host device to reset the processor (i.e., USB reset, see col. 2, lines 42-50).

Re claim 23: Feuser discloses a smart card apparatus (see Figs. 1 and 2), comprising: a processor (i.e., CPU; See col. 1, line 60); a device controller (i.e., smart card controller Core K in Fig. 1) that can perform register-based (i.e., ISO standard compliant) and interrupt-based (i.e., USB standard compliant) communication with the processor (see col. 4, lines 15-19), the device controller including: a status register (i.e., status register in Fig. 2) coupled to the processor to store status information indicative of a status associated with the processor (see col. 3, lines 1-9 and 44-47); and control logic (i.e., internal reset circuit in Fig. 2), wherein the control logic (i.e., the internal reset circuit) can initiate a reset signal, see col. 2, lines 25-31).

Feuser does not expressly teach the control logic is coupled to the processor and to the status register to check the status information stored therein to determine the status of the processor, and wherein if the control logic determines that the status information indicates a non-responsive state associated with the processor, the control logic can initiate the reset signal to the processor to remove the processor from the non-responsive state.

Poisner discloses an apparatus for automatically selecting CPU clock frequency multiplier (See Abstract), wherein a system logic device comprising a control logic (i.e., processor failure detection unit 284 in Fig. 2) is coupled to a processor (i.e., coupled to processor 210 via system bus 225 in Fig. 2) and to a status register (i.e., clock frequency multiplier indicator circuit 285 and non-volatile memory device 270 in Fig. 2) to check a status information stored therein to determine a status of the processor (see col. 3,

lines 6-9 and 17-19; in fact, the processor failure detection unit checks to see the processor status if it performs a first instruction fetch from the non-volatile memory device inherently implies a control logic coupled to a processor and to a status register to check a status information stored therein to determine a status of the processor), and wherein if the control logic determines that the status information indicates a non-responsive state associated with the processor (i.e., processor failure is detected, see col. 4, lines 45-47), the control logic (i.e., the processor failure detection unit) can initiate the reset signal (i.e., reset 201 in Fig. 2) to the processor to remove the processor from the non-responsive state (i.e., resetting the processor with making a determination of whether the processor is behaving properly, see col. 3, lines 61-64).

Therefore, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to have included the system logic device, as disclosed by Poisner in the control logic (i.e., internal reset circuit), as disclosed by Feuser, for the advantage of providing the smart card (i.e., device) for selecting a clock frequency multiplier without the need of human intervention (see col. 2, lines 60-64 of Poisner).

Re claim 24: Feuser teaches the control logic (i.e., internal reset circuit in Fig. 2) can initiate the reset signal (i.e., RST, see col. 2, lines 36-41) and a current configuration and state of the device controller (i.e., smart card controller Core K in Fig. 1) is maintained (i.e., the smart card controller K maintains its configuration based on the detected standard, such that ISO compliant or USB compliant, see col. 4, lines 40-47).

Re claim 27: Feuser as modified by Poisner teaches the device controller (i.e., smart card controller Core K in Fig. 1) comprises part of an USB-compliant smart card (see col. 1, lines 50-56), and wherein the non-responsive state comprises a mute mode (i.e., processor failed status, which means no operation may be performed, see col. 4, lines 50-52).

Allowable Subject Matter

3. Claims 5-8, 10-11, 15-16, 19, 21-22, and 25-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. The following is a statement of reasons for the indication of allowable subject matter: The prior art of the record fails to teach or fairly suggest the followings within the smart card apparatus: a vendor specific request (VSR) block, having an output terminal coupled to a first input terminal of the control logic, to decode a received VSR and to provide a corresponding VSR signal to the control logic to allow the control logic to generate the second input signal in response thereto; the specifics of the claimed signal lines in relation of the processor, the status register, control logic for specific responses of non-responsive states; the specifics of the claimed communicating lines in relation of the processor and external receiving device for specific responses of routing and for buffering the received external information; and the specifics steps of checking the status information (i.e., instructions to regularly polling a data repository and review the status information after it has been updated in response to a change in status resetting operation (i.e., steps of setting bit prior to the processor's entry into the non-responsive state, updating and clearing steps of non-responsive state), and steps of bit setting to indicate the non-responsive state, as set forth in the claims.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Fruhauf [WO 02/31761], Drabczuk et al. [US 2003/0093609], Rhelimi [US 4,840,464], and Lee [US 2002/0011516] disclose a smart card interface with a USB. .

Any inquiry concerning this communication or earlier communications from the examiner should be directed to D. I. Lee whose telephone number is (571) 272-2399. The examiner can normally be reached on Monday through Thursday from 5:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G. Lee can be reached on (571) 272-2398. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D. I. Lee
Primary Examiner
Art Unit 2876

D. L.